Amendments to the Specification:

Please amend the paragraph beginning on page 18, line 4 in the following manner:

-- Figures 6a to 6e provide an outline illustration of a number of method steps used to fabricate a semiconductor chip illustrated in Figure 1a. In Figure 6a, a growth substrate wafer 10, which consists, for example, of SiC, is provided and the n-conducting semiconductor layer 11 is deposited epitaxially on the growth substrate wafer 10. Then, the active region 12 and the p-conducting semiconductor layer 13 are grown epitaxially. The deposition conditions (for example the deposition temperature, deposition time, doping level) are selected in such a way that pyramid-like structures whose sub-surfaces form the desired angles [[(]] with the main plane, namely between 10° and 50°, are formed on the p-conducting semiconductor layer ~~11~~ 13.

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